(12) UK Patent Application (19) GB (11) 2 356 540 (13) A

(43) Date of A Publication 23.05.2001

(21) Application No 0018759.1

(22) Date of Filing 31.07.2000

(30) Priority Data
(31) 99031587 (32) 31.07.1999 (33) KR

(71) Applicant(s)
LG Electronics, Inc.
(Incorporated in the Republic of Korea)
20 Yoido-Dong, Youngdungpo-Gu, Seoul,
Republic of Korea

(72) Inventor(s)
Woong Gyu Kim

(74) Agent and/or Address for Service
Kilburn & Strode
20 Red Lion Street, LONDON, WC1R 4PJ,
United Kingdom

(51) INT CL[7]
G06F 3/147 // G06F 12/06

(52) UK CL (Edition S)
H4T TBAX T113 T114

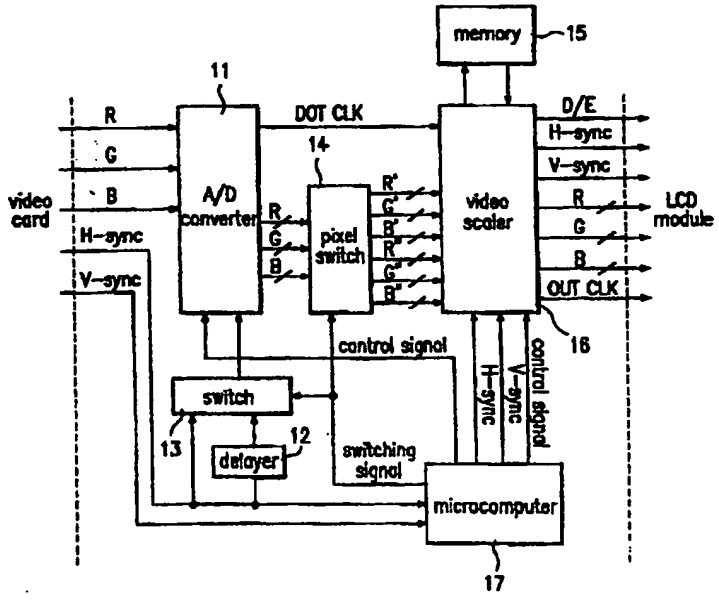
(56) Documents Cited
None

(58) Field of Search
UK CL (Edition S) H4T TBAX TBBX TBCX
ONLINE: WPI; JAPIO; EPODOC; COMPUTER

(54) Abstract Title
Display means capable of displaying input signals that exceed a monitor's maximum resolution

(57) An image display device and method for a monitor is provided, which can provide a normal display even when the resolution of input signals exceeds that supported by the monitor. The device includes an A/D converter (11) to produce signals according to a sampling clock; a delayer (12); a switch (13) to generate the sampling clock according to a switching signal; a memory; a video scaler (16) for storing the signals in the memory to build one frame and to transmit the stored output to match a signal input timing of a display module; and a microcomputer (17) to output a switching signal to switch the switch, if the input image resolution exceeds that supported by the monitor, and to output a control signal to set the sampling clock to half a normal sampling clock.

FIG.2



GB 2 356 540 A

FIG.1

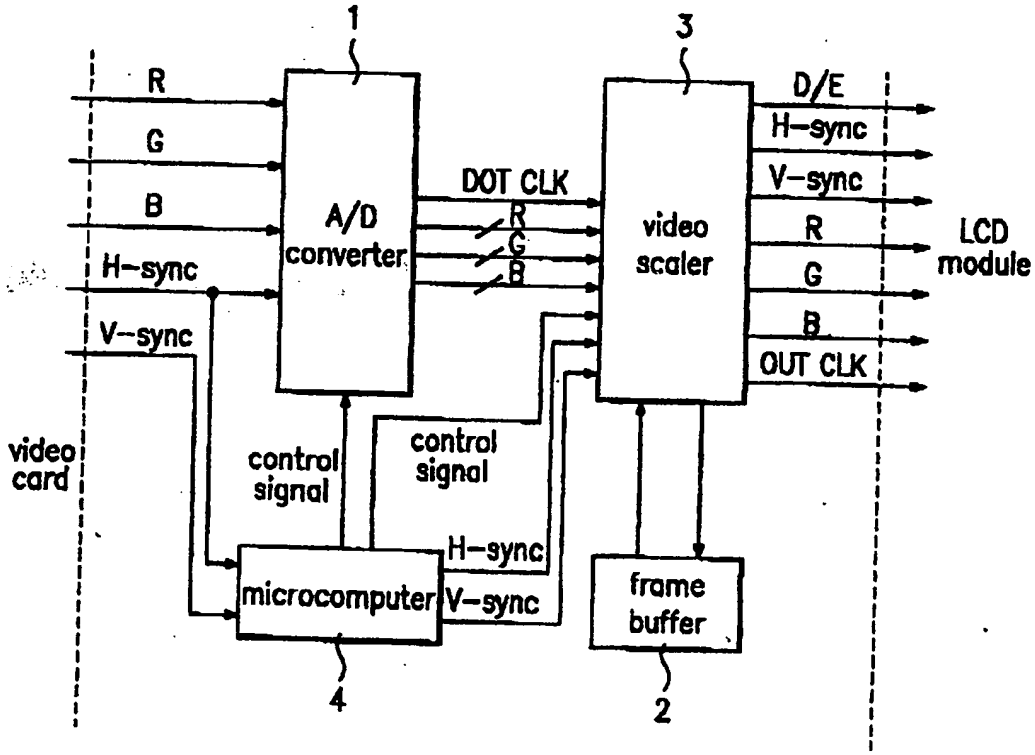

1
3
R
G
B
H-sync
V-sync
A/D converter
DOT CLK
R
G
B
video scaler
D/E
H-sync
V-sync
R
G
B
OUT CLK
LCD module
video card
control signal
control signal
H-sync
V-sync
microcomputer
frame buffer
4
2

FIG.2

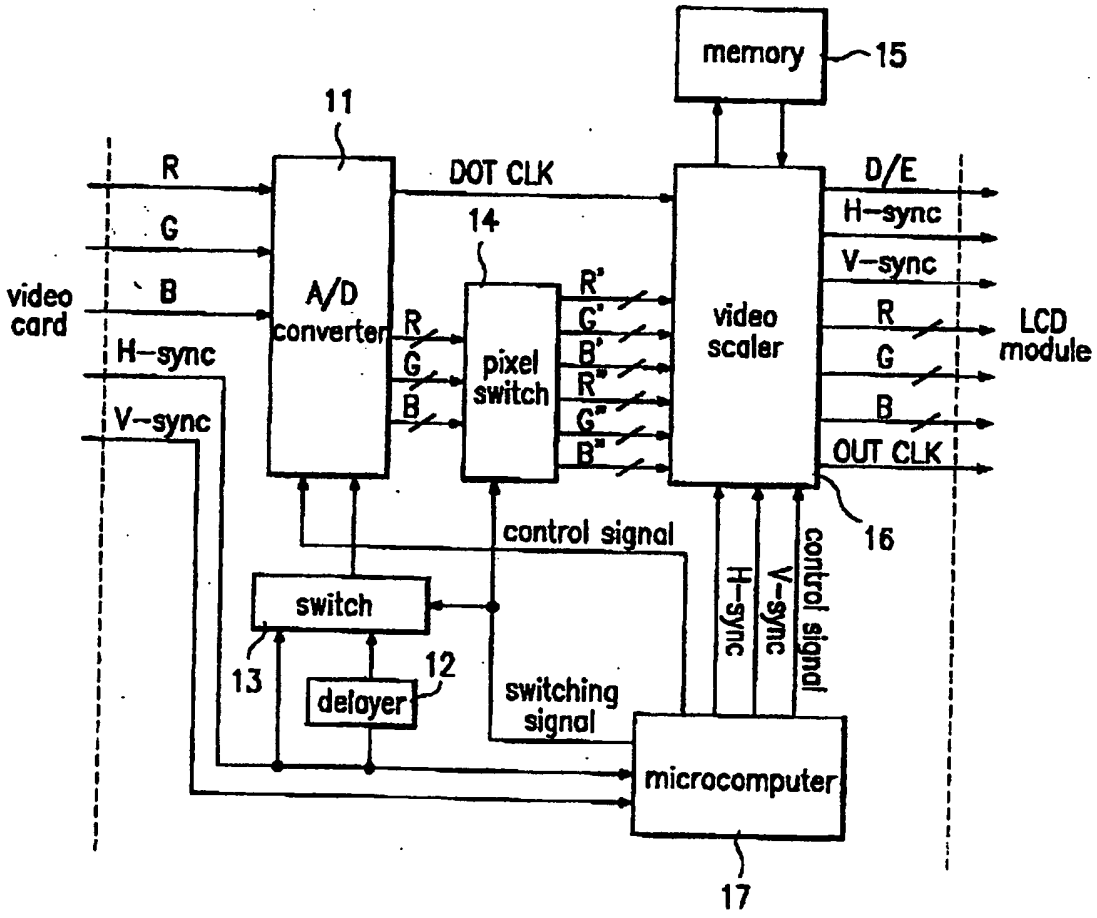

memory
15
11
R
G
B
video card
H-sync
V-sync
A/D converter
DOT CLK
14
R
G
B
pixel switch
R'
G'
B'
R''
G''
B''
video scaler
D/E
H-sync
V-sync
R
G
B
OUT CLK
LCD module
16
control signal
switch
13
delayer
12
switching signal
H-sync
V-sync
control signal
microcomputer
17

FIG.3

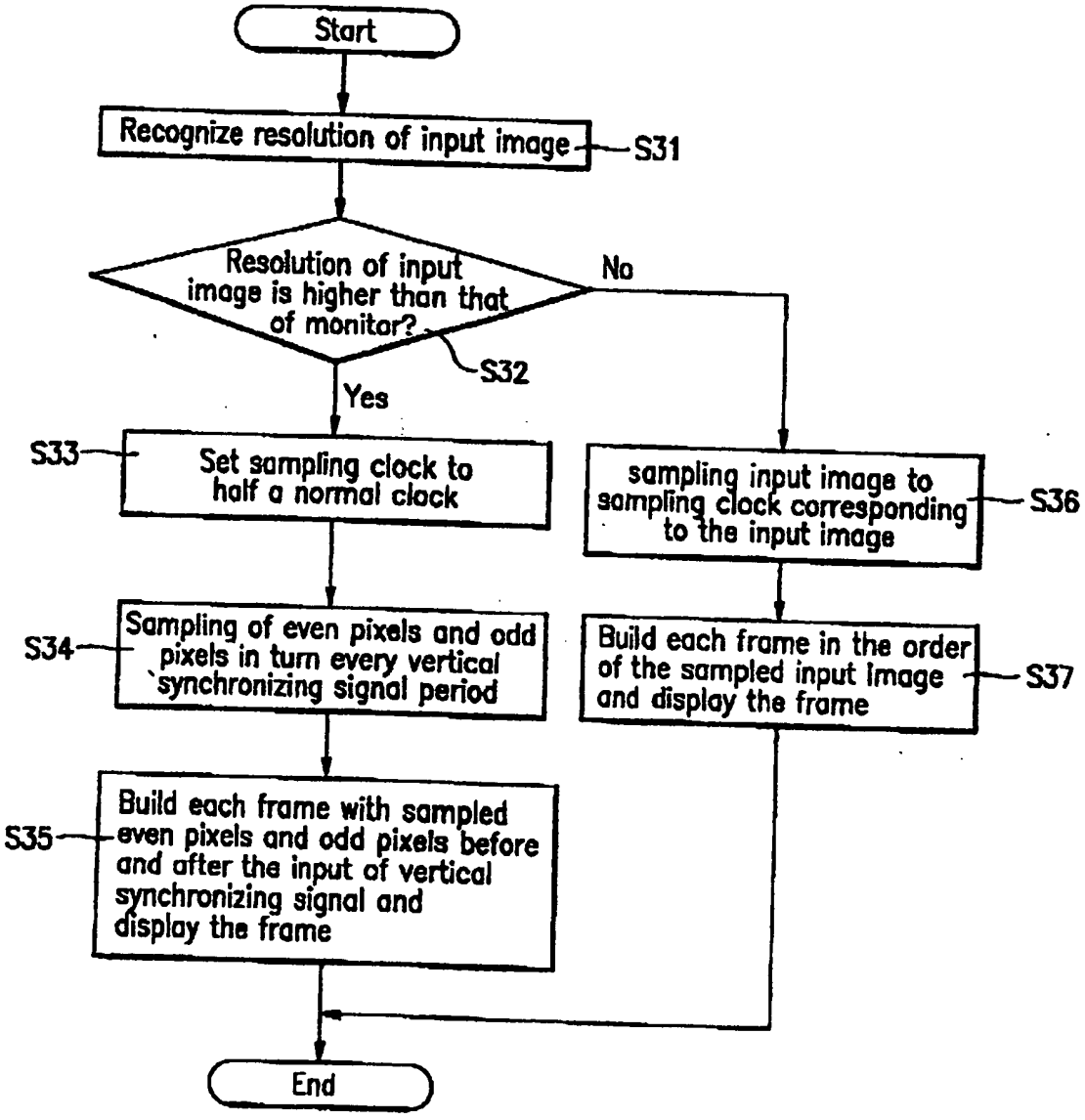
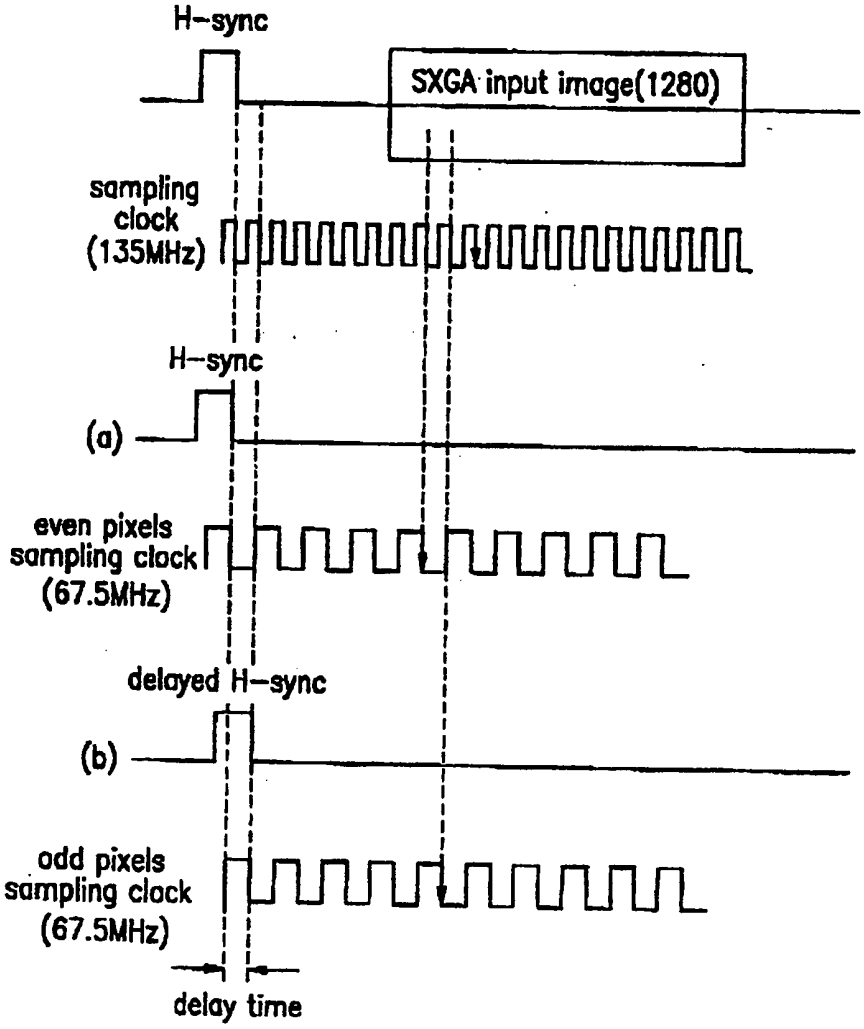

Start
Recognize resolution of input image
S31
Resolution of input image is higher than that of monitor?
S32
No
Yes
S33
Set sampling clock to half a normal clock
S34
Sampling of even pixels and odd pixels in turn every vertical synchronizing signal period
S35
Build each frame with sampled even pixels and odd pixels before and after the input of vertical synchronizing signal and display the frame
sampling input image to sampling clock corresponding to the input image
S36
Build each frame in the order of the sampled input image and display the frame
S37
End

FIG.4


H-sync
SXGA input image(1280)
sampling clock (135MHz)
H-sync
(a)
even pixels sampling clock (67.5MHz)
delayed H-sync
(b)
odd pixels sampling clock (67.5MHz)
delay time

OUT OF RANGE IMAGE DISPLAYING DEVICE AND METHOD OF MONITOR

The present invention relates to an out of range displaying device and method for a monitor.

A monitor typically executes a series of signal processing operations, such as digital sampling, scaling, and the like for image signals of a predetermined format transmitted from a source, such as a video card of a personal computer connected to the monitor. The monitor then displays the processed image signals on a screen.

Large display devices are presently under development using current technology. Accordingly, the monitor has progressed from a small monitor using a cathode-ray tube into a digital system using a liquid crystal display (LCD) as a representative flat display device adequate for the large monitor.

The image display performance of the monitor is determined by its resolution, which is divided into SVGA (800 x 600), XGA (1024 x 768) and SXGA (1280 x 1024).

As shown in Figure 1, an image processing device of a monitor in the prior art includes an A/D converter 1 for converting analog R, G, and B image signals transmitted

from a video card into 8-bit digital R, G, and B image signals according to a predetermined sampling clock, which is synchronous with a horizontal synchronizing signal H-sync controlled by a control signal of a microcomputer 4. A buffer 2 is further provided for temporarily storing the digital R, G, and B image signals in a frame unit, and a video scaler 3 converts the digital R, G, and B image signals outputted from the A/D converter 1 into the signals in a frame unit, which can be displayed on an LCD module. The converted image signals are stored in the frame buffer 2 and transmitted so as to match an input timing signal of the LCD module. Finally, microcomputer 4 recognizes an input image format in accordance with horizontal and vertical synchronizing signals H-sync and V-sync transmitted from the video card, and outputs the control signal to both the A/D converter 1 and the video scaler 3, so as to match the display with the corresponding format.

In operation, if the analog R, G, and B image signals and the horizontal and vertical synchronizing signals are inputted from the video card, the microcomputer 4 first recognizes the resolution of the inputted image signals, namely, SVGA, XGA and SXGA by using the horizontal/vertical synchronizing signals.

Then, the microcomputer 4 applies the control signal to set the sampling clock of the A/D converter 1 for the digital conversion. The sampling clock is set to correspond to the resolution set by a user, in case where the resolution of the input image signals is below the resolution supported in the monitor, for example, when the resolution of the

monitor is XGA (1024 x 768) and the resolution of the input image signals is XGA or VGA.

In response to the control signal, the A/D converter 1 generates the sampling clock of 95MHz to sample the XGA image signals to match with the horizontal synchronizing signal timing. It also executes the digital sampling for the input image signals, and outputs the 8-bit digital R, G, and B image signals. At the same time, the A/D converter 1 outputs a dot clock Dot Clock for recognizing the signal of the video scaler 3.

The video scaler 3 then stores the output of the A/D converter 1 in a frame unit, matching the resolution of XGA in the frame buffer 2, and outputs the stored output to the LCD module, in accordance with the control signal of the microcomputer 4.

The LCD module recognizes the 8-bit digital R, G, and B image signals outputted from the video scaler 3 according to a data enable signal D/E and an external clock OUT CLK, and displays the image signals to corresponding to the horizontal/vertical synchronizing signals.

When, however, the resolution of the monitor is XGA and the resolution of the input image signals is SXGA thus exceeding the display performance of the monitor, a sampling clock rate of 135MHz is required to convert the SXGA image signals into the digital signals.

When the monitor has a resolution of XGA, it can only generate a maximum sampling clock rate of 100MHz. It thus fails to display the input image signals on the screen, and instead displays the "out of range" on screen display (OSD).

Since the prior art monitor cannot display the input image when the input image signals are out of range of the monitor, a problem arises in that the monitor should be replaced by a new monitor that supports the input image mode in order for a user to view the corresponding image.

An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

Another object of the present invention to provide an out of range image displaying device and method for a monitor capable of achieving a normal display even when the resolution of input image signals exceeds the resolution supported by the monitor.

Another object of the present invention is to provide a device and method of displaying video data having a first format on a monitor having a second format.

The present invention is set out in the independent claims. Some optional features are set out in the claims dependent thereto.

According to one embodiment, there is provided an out of range image displaying device for a monitor, which includes an A/D converter for converting analog image signals into digital image signals composed of even pixels, odd pixels, and even/odd pixels in accordance with a sampling clock set by a control signal; a delayer for delaying a horizontal synchronizing signal for a predetermined time; a switch for selecting one of the horizontal synchronizing signal delayed for the predetermined time by the delayer and a normal horizontal synchronizing signal to generate the sampling clock of the A/D converter in accordance with a switching signal; a memory for temporarily storing the digital image signals in a frame unit; a video scaler for storing the even and odd pixels digital image signals outputted from the A/D converter in the memory to thereby build one frame for transmitting the stored output to match with a signal input timing of a display module; and a microcomputer for outputting the switching signal to switch the switch in synchronism with the vertical synchronizing signal, if the resolution of the input image is over the resolution supported by the monitor and at the same time to output the control signal for setting the sampling clock of the A/D converter to half a normal sampling clock.

According to a further embodiment, there is provided an out of range image displaying method for a monitor, which includes determining whether the resolution of external input image signals is out of range of the resolution supported by the monitor; and if the resolution of external input image is out of range of that supported by the monitor, sampling

even or odd pixels for each of the image signals inputted before and after the input of a vertical synchronizing signal; and building each frame with the even and odd pixels sampled in the image signals inputted before and after the input of the vertical synchronizing signal and displaying the frame.

According to yet a further embodiment,

there is provided an image displaying device that includes an A/D converter to convert image signals of a first format into image signals of a second format, a pixel switch that divides the digital image signal into a plurality of first pixels and a plurality of second pixels, a delay circuit to delay a horizontal synchronizing signal for a prescribed period of time, a switch to select one of the horizontal synchronizing signal and a delayed horizontal synchronizing signal in accordance with a switching signal, a video scaler to build a frame from at least one of the first and second pixels of the digital image signals outputted from the pixel switch.

According to one embodiment,

there is provided a method of displaying images on a monitor that includes determining whether the resolution of external input image signals exceeds that of the monitor, setting a sampling clock, sampling even or odd pixels for each of the image signals inputted before and after the input of a vertical synchronizing signal, and building each frame using at least one of the even and odd pixels sampled in the image signals

inputted before and after the input of the vertical synchronizing signal and displaying the frame.

According to yet another embodiment, there is provided an image display and method for a monitor which can provide a normal display, even when the resolution of input signals exceeds that supported by the monitor. The displaying device includes an A/D converter for converting analog image signals into digital image signals composed of even pixels, odd pixels and even/odd pixels in accordance with a sampling clock set by a control signal; a delayer for delaying a horizontal synchronizing signal delayed for the predetermined time; a switch for selecting one of the horizontal synchronizing signal delayed for the predetermined time by the delayer and a normal horizontal synchronizing signal to generate the sampling clock of the A/D converter in accordance with a switching signal; a memory for temporarily storing the digital image signals in a frame unit; a video scaler for storing the even and odd pixels digital image signals outputted from the A/D converter in the memory to thereby build one frame and to transmit the stored output to match a signal input timing of a display module; and a microcomputer to output a switching signal to switch the switch in synchronism with the vertical synchronizing signal, if the resolution of the input image is over the resolution supported by the monitor, and at the same time to output a control signal to set the sampling clock of the A/D converter to half a normal sampling clock.

The present invention can be put into practice in several ways. Specific embodiements are now described by way of example by reference to the accompanying drawings, in which like reference numerals refer to like elements, and in which:

Figure 1 is a block diagram illustrating the configuration of a prior art image processing device for a monitor;

Figure 2 is a block diagram illustrating the configuration of an out of range image displaying device for a monitor according to a preferred embodiment of the present invention;

Figure 3 is a flowchart illustrating an out of range image displaying method for a monitor according to a preferred embodiment of the present invention; and

Figure 4 is a timing diagram illustrating the waveforms of the horizontal synchronizing signal and the sampling clock according to a preferred embodiment of the present invention.

The configuration and operation of an out of range image displaying device and method for a monitor as embodied and broadly described according to the present invention will be hereinafter described with reference to Figures 2, 3, and 4.

Referring to Figure 2, an out of range image displaying device for a monitor according to the preferred embodiment includes an A/D converter 11 for converting analog R, G, and B image signals transmitted from a video card into 8-bit digital R, G, and B image signals. The digital R, G, and B image signals are preferably composed of even pixels, odd pixels, and even/odd pixels, in accordance with a sampling clock set by a control signal of a control circuit 17, such as a microcomputer.

Next, a delay circuit 12 delays a horizontal synchronizing signal for a prescribed period of time, and a switch 13 selects one of the delayed horizontal synchronizing signal and the normal horizontal synchronizing signal. The switch 13 transmits the selected signal as a timing signal for generating the sampling clock of the A/D converter 11 in accordance with a control signal of the microcomputer 17.

A pixel switch 14 is further provided to output the even pixels and odd pixels of the 8-bit digital R, G, and B image signals, which are outputted sequentially from the A/D converter 11, to each path in accordance with a control signal of the microcomputer 17. A video scaler 16 stores the even and odd pixels 8-bit digital R, G, and B image signals outputted to each path through the pixel switch 14 to build one frame in the frame buffer 15, which temporarily stores the digital R, G, and B image signals in a frame unit. The video scaler 16 then transmits the stored image signals to match with a signal input timing of an LCD module.

The microcomputer 17 recognizes the resolution of the input image according to the horizontal and vertical synchronizing signals transmitted from the video card, and if the resolution of the input image is higher than the resolution supported by the monitor outputs the control signal for switching the switch 13 and the pixel switch 14 in synch with the vertical synchronizing signal. At the same time, it outputs a control signal for setting the sampling clock of the A/D converter 11 to half a normal sampling clock.

Under the above construction, a description of an out of range image displaying method for a monitor according to a preferred embodiment of the present invention will be described.

Referring to Figure 3, if the analog R, G, and B image signals and the horizontal and vertical synchronizing signals are inputted from the video card, the microcomputer

17 recognizes the resolution of the input image signals, that is, SVGA, XGA or SXGA by using the horizontal/vertical synchronizing signals (Step S31).

Then, the microcomputer 17 determines whether the resolution of the input image signals is higher than the resolution supported in the monitor (Step S32).

If it is determined that the resolution of the input image signals is higher than the resolution supported in the monitor, for example, if the resolution of the monitor is XGA (1024 x 768) and that of the input image signals is SXGA (1280 x 1024), the microcomputer 17 outputs the control signal to the A/D converter 11 and sets the sampling clock to half a normal sampling clock of 135MHz required for converting the SXGA image to the digital signals, that is, to the clock of 67.5MHz (Step S33).

Next, the A/D converter 11 samples the even pixels of the input image to build a first frame, according to the sampling clock of 67.5MHz, synchronized with the horizontal synchronizing signal at an original state, as shown in "(a)" in Figure 4 and converts the input image signals into the 8-bit digital R', G', and B' image signals.

If the vertical synchronizing signal is inputted, the A/D converter 11 executes the sampling for the odd pixels of the input image to build a second frame, according to the sampling clock of 67.5MHz synchronized with the horizontal synchronizing signal delayed for a prescribed time, as shown in "(b)" in Figure 4, and converts the input image signals into the 8-bit digital R", G", and B" image signals (Step S34). At this time, if the image signals for building the first frame are inputted, the microcomputer 17 controls the

switch 13 under the output of the switching signal and inputs the horizontal synchronizing signal at the original state to the A/D converter 11.

If the vertical synchronizing signal is inputted and the image signals for building the second frame are then inputted, the microcomputer 17 controls the switch 13 under the output of the switching signal and inputs to the A/D converter 11, the delayed horizontal synchronizing signal, which is delayed in the delayer 12 for the prescribed time required for sampling the odd pixels, for example, for the half period the sampling clock of 67.5MHz.

Since the pixel switch 14 and the switch 13 switch according to the same switching signal, the pixel switch 14 transmits the R', G', and B' image signals and the R", G", and B" image signals to the video scaler 16 via each path of the image signals.

The video scaler 16 stores the R', G', and B' image signals in the memory corresponding to the even pixels in the frame buffer 15 and the R", G", and B" image signals in the memory corresponding to the odd pixels in the frame buffer 15, so as to build one frame, and outputs the built frame to the LCD module. It thus displays the output (Step S35).

In other words, for a normal display, the sampling for only the even pixels in the image corresponding to the first frame of the image corresponding to two frames and for only the odd pixels in the image corresponding to the second frame is carried out to build one frame, thereby displaying the one frame.

The two frames are then synthesized on the normal display process to build the one frame, but a viewer cannot sense the abnormal state of the screen due to the afterglow effect of the LCD screen, such that it appears as a normal display.

On the other hand, if the resolution of the input image signals is below the resolution supported in the monitor, for example, if the resolution of the input image signals is XGA (1024 x 768), then the A/D converter 11 executes the sampling for the input image with the sampling clock of 95MHz corresponding to the resolution and converts the input image into the 8-bit digital image signals (Step S36).

The microcomputer 17 then sets the sampling clock of the A/D converter 11 to 95MHz in accordance with the control signal thereof, and controls the switch 13 in accordance with the output of the switching signal. The horizontal synchronizing signal is thereby inputted at the original state to the A/D converter 11, regarless of the input of the vertical synchronizing signal.

Finally, each frame is built with the sampled digital image signals in a sequential order and displayed through the LCD module (Step S37).

As clearly apparent from the foregoing, an out of range image displaying device and method for a monitor according to the present invention is capable of achieving a normal display even in case where the resolution of input image signals exceeds the resolution supported by the monitor, thereby removing a problem that the monitor should be exchanged and improving the reliability of the product for a user.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.

CLAIMS:

1. An image displaying device, comprising:

an A/D converter to convert image signals of a first format into image signals of a second format;

a pixel switch that divides the digital image signal into a plurality of first pixels and a plurality of second pixels;

a delay circuit to delay a horizontal synchronizing signal for a prescribed period of time;

a switch to select one of the horizontal synchronizing signal and a delayed horizontal synchronizing signal in accordance with a switching signal; and

a video scaler to build a frame from at least one of the first and second pixels of the digital image signals outputted from the pixel switch.

2. The device of claim 1, wherein the prescribed delay is a half period of a sampling clock of said A/D converter.

3. The device of claim 1, wherein the pixel switch outputs each of the pixels of the image signals of the second format, which were outputted sequentially from said A/D converter, to each corresponding path of said video scaler in accordance with a control signal of a control circuit.

4. The device of claim 3, wherein the corresponding paths of said video scaler are paths for outputting even pixels and odd pixels of the image signals of the second format to an even pixel input terminal at which the even pixels are inputted and an odd pixel input terminal at which the odd pixels are inputted,

respectively.

5. The device of claim 3, wherein said pixel switch performs its switching according to the same control signal as said switch.

6. The device of claim 1, further comprising a control circuit, which outputs the switching signal to switch said switch in synchronism with a vertical synchronizing signal, if the resolution of the input image is higher than a resolution supported by the monitor, and which simultaneously outputs a control signal to set a sampling clock of said A/D converter to half a normal sampling clock.

7. The device of claim 1, wherein the plurality of first pixels comprise even pixels of the image signal of the second format, and the plurality of second pixels comprise odd pixels of the image signal of the second format.

8. The device of claim 1, wherein the A/D converter converts the image signals in accordance with a sampling clock set by a control signal, which is set by a control circuit.

9. The device of claim 1, wherein the first format is analog and the second format is digital.

10. An image displaying device for a monitor, comprising: a signal generator to generate an image signal, a horizontal synchronizing signal and a vertical synchronizing signal; a control circuit to determine an image signal resolution; an A/D converter to convert the image signal from a first to a second format

according to a normal clock rate of a sampling clock; and a video scaler to build a frame from the second format signals; in which when the determined image signal resolution is greater than a maximum monitor resolution, the control circuit outputs a control signal to change the normal clock rate.

11. A device as claimed in claim 10, further including a delay circuit to delay one of the horizontal synchronizing signals; a switch to select one of the horizontal synchronizing signals, and a delayed horizontal synchronizing signal; and a pixel switch to divide the digital image signal into a plurality of pixels; in which when the determined image resolution is greater than a maximum monitor resolution, the control circuit outputs a control signal so that the switch and the pixel switch operate in synchronism with the vertical synchronizing signal.

12. A device as claimed in claim 10 or claim 11 in which the changed clock rate is half the normal clock rate.

13. A method of displaying images on a monitor, comprising: generating an image signal, a horizontal synchronizing signal and a vertical synchronizing signal; converting the image signal from a first to a second format according to a normal clock rate of a sampling clock; building a frame from the second format signals; determining whether an image signal resolution exceeds a maximum monitor resolution; and changing the normal clock rate according to the determined image signal resolution.

14. A method as claimed in claim 13 further including delaying at least one of the horizontal synchronizing signals; selecting one of the horizontal

synchronizing signals and a delayed synchronizing signal; dividing the digital image into a plurality of pixels; and outputting a signal to synchronize the switching step and the dividing step, with the vertical synchronizing signal.

15. A method of displaying images on a monitor, comprising:

determining whether the resolution of external input image signals exceeds that of the monitor;

setting a sampling clock;

sampling even or odd pixels for each of the image signals inputted before and after the input of a vertical synchronizing signal; and

building each frame using at least one of the even and odd pixels sampled in the image signals inputted before and after the input of the vertical synchronizing signal and displaying the frame.

16. The method of claim 15, wherein said sampling step further comprises:

sampling the even pixels of the input image before the input of the vertical synchronizing signal; and

sampling the odd pixels of the input image after the input of the vertical synchronizing signal.

17. The method of claim 15, wherein said sampling step further comprises:

sampling the odd pixels of the input image before the input of the vertical synchronizing signal; and

sampling the even pixels of the input image after the input of the vertical synchronizing signal.

18. The method of claim 15, wherein said sampling clock setting step

comprises setting the sampling clock to half a normal sampling clock for sampling the whole image.

19. The method of claim 15, further comprising sampling the input image with a sampling clock corresponding to the resolution, and building each frame with the image signals sampled in a sequential order and displaying the frame.

INVESTOR IN PEOPLE

Application No:	GB 0018759.1	**Examiner:**	Frank D. Moeschler
Claims searched:	1-9	**Date of search:**	16 March 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H4T (TBAX, TBBX, TBCX)

Int Cl (Ed.7):

Other: Online: WPI; JAPIO; EPODOC; COMPUTER

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
	None found	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.